AMENDMENTS TO THE SPECIFICATION:

Under "Related Applications", please amend the paragraph beginning on page 1, line 8 as follows:

Related Applications

This application is a continuation of U.S. Serial No. 10/236,408; filed September 5, 2002; which is a continuation application of U.S. Serial No. 09/386,170; filed August 31, 1999; which is a continuation application of U.S. Serial No. 09/207,956; filed December 9, 1998; now U.S. Patent No. 6,002,152; issued December 14, 1999; which is a continuation application of U.S. Serial No. 08/908,744; filed August 7, 1997; now U.S. Patent No. 5,883,409; issued March 16, 1999; which is a divisional of U.S. Serial No. 08/607,951; filed February 28, 1996; now U.S. Patent No. 5,712,180; issued January 27, 1998. ~~is a continuation in part of U.S. Serial Number 08/193,707 filed February 9, 1994, which in turn is a divisional of U.S. Serial Number 07/820,364, filed January 14, 1992, now U.S. Patent 5,313,421 issued May 17, 1994.~~

Under "Background", please amend the paragraph beginning on page 3, line 33 as follows:

In view of these benefits, ~~SunDisk~~ SanDisk Corporation has patented FLASH memory cell and array variants which use source side injection integrated with ~~SunDisk's~~ SanDisk's proprietary thick oxide, poly-to-poly erase tunneling technology, to make a highly scalable, reliable, low power programming cell (D.C. Guterman, G. Samachiasa, Y. Fong and E. Harari, U.S. Patent No. 5,313,421).

Under "Description of Specific Embodiments" please amend the paragraph beginning on page 10, line 24 as follows:

An example of operating conditions and levels associated with the embodiment of Fig. 1b are shown in Table 1. High efficiency programming comes about by the ability to

simultaneously create a high field region in channel 106-2 under the floating gate, which under the bias conditions of Table 1 occur near the gap between channels 106-1 and 106-2 (see above mentioned IEDM article of Kamiya for theory) while maintaining a low ~~channel/current~~ channel current. Since this high field causes electron injection to floating gate 107 near the source side of channel 106-2, this type of operation is termed "source-side" injection. This mechanism provides high efficiency, low power programming by maintaining a low channel current via word line 109 throttling by using a bias operating near channel threshold, VT_{p3}. A major attribute of this type of operation is that it allows for a high drive condition in floating gate channel 106-2 under the floating gate (in fact it thrives on it), offering high-performance read, without degrading programming performance. This is because the very weak drive condition on the select transistor of channel 106-1 is established via the throttling mentioned above to achieve the high fields in the vicinity of the poly 3/poly 1 gap. These fields accelerate the electrons to sufficiently energetic levels (i.e. > 3.1 eV) to surmount the Si/SiO_2 interface barrier at the source side of floating gate 107. Furthermore, there is a significant vertical component to that field (i.e. normal to the Si/SiO_2 surface) driving the electrons up to the surface of channel 106, and thereby assisting the injection into floating gate 107. No read performance penalty is incurred to establish this high field condition. This is in stark contrast to conventional drain side programming, wherein efficient program requires strong channel saturation which shuns high floating gate channel drives, strong overerase, or a weakly turned on series select transistor. These problems with drain side programming dictate high channel currents, care in overerase, potentially high drain voltages, and unfavorable fields (potentially subducting the channel below the surface at the drain side and driving electrons downward away from the floating gate).

Under "Description of Specific Embodiments" please amend the paragraph beginning on page 12, line 4 (at line 10) as follows:

TABLE 1

State Table & Operating Conditions (Fig. 1b)

~~Node~~ Mode of Operation	Poly 3 (Word line)	Poly 2 (Steering Gate)	Drain (BN & Drain)	Source & (BN Source)
R STANDBY	0v	0v	1.0v or 0v	1.0v or 0v
E L READ SELECTED	5v	0v	1.0v or 0v	0v or 1.0v
A T READ UNSELECTED	5v	0v	1.0v	1.0v
D E D				
E R ERASE UNSELECTED	5v	0v	0v	0v
R E A L S A E T ERASE Option 1	5v	-10to-17v	0v	0v
E D or Option 2	12-22v	0v	0v	0v
P R PROGRAM	H1.5v	14-20v	5-7v	0v
R E SELECTED				
O L G A				
R T PROGRAM	0v	14-20v	5-7v	0v
A E UNSELECTED	H1.5V	14-20v	5-7v	5-7v
M D	0v	14-20v	0v	0v

Under "Description of Specific Embodiments" please amend the paragraph beginning on page 23, line 1 (at lines 6 and 17) as follows:

TABLE 3

State Table & Operating Conditions (Fig. 2a)

~~Node~~ Mode of Operation	Poly 3 (Word line)	Poly 2 (Steering Gate)	Drain	Source
R R STANDBY	0v	0v	Don't care	0v
E E READ SELECTED	5v	0v	2.5v	0v
A L READ UNSELECTED	5v	0v	Don't care	0v
D A T E D				
E R ~~STANDBY~~ ERASE UNSELECTED				
R E	0v	0v	0v	0v
A L S A E T ERASE Option 1	12v-22v	0v	0v	0v
E D Option 2	5v	-10v to -12v	0v	0v
P R PROGRAM	H1.0v	14-20	0v	5v-8v
R E SELECTED O L G A				
R T PROGRAM	0v	14-20	0v	5v-8v
A E UNSELECTED	H1.0v	14-20	5v	5v-8v
M D	0v	14-20	5v	5v-8v

Under "Description of Specific Embodiments" please amend the paragraph beginning on page 24, line 1 as follows:

Various embodiments of a process suitable for fabricating a structure in accordance with the embodiment of Figures 1a-1d are now described. Reference can also be made to copending U.S. Application Serial No. 323,779 filed March 15, 1989 (now U.S. Patent 5,070,032), and assigned to ~~SunDisk~~ SanDisk, the assignee of this invention. Reference may also be made to fabrication process steps described earlier in this application. A starting

substrate is used, for example a P type substrate (or a P type well region within an N type substrate). A layer of oxide is formed, followed by a layer of silicon nitride. The layer of silicon nitride is then patterned in order to expose those areas in which N+ source and drain regions are to be formed. The N+ source and drain regions are then formed, for example, by ion implantation of arsenic to a concentration of approximately $1x10^{20}cm^{-3}$. The wafer is then oxidized in order to form oxide layers 104 and 105 in order to cause source and drain regions 102 and 103 to become "buried". Note that for the embodiment of Figure 2a, this oxidation step is not utilized, as the source and drain regions are not "buried". Rather, the source and drain regions are formed after all polycrystalline silicon layers are formed, in a conventional manner. The remaining portion of the nitride mask is then removed, and the oxide overlying channel regions 106-1 and 106-2 is removed. A new layer of gate oxide overlying channel regions 106-1 and 106-2 is formed, for example to a thickness within the range of 150Å to 300Å and implanted to the desired threshold (e.g. approximately -1v to +1v). Polycrystalline silicon is then formed on the wafer and patterned in order to form floating gate regions 107. If desired, the polycrystalline silicon layer is patterned in horizontal strips (per the orientation of Figure 1a), with its horizontal extent patterned at the same time as the patterning of the second layer of polycrystalline silicon, as will be now described. Following the formation polycrystalline silicon layer 107 at this time, a layer of oxide or oxide/nitride dielectric is formed over the remaining portions of polycrystalline silicon layer 107. A second layer of polycrystalline silicon 108 is then formed and doped to a desired conductivity, for example 30 ohms/square. The second layer of polycrystalline silicon is then patterned into vertical strips (again, per the orientation of Figure 1a). If the horizontal extent of polycrystalline silicon layer 107 was not earlier defined, this pattern step is also used to remove the layer of dielectric between the first and second layers of polycrystalline silicon in those areas where the first layer of polycrystalline silicon is to be patterned simultaneously with the patterning of the second layer of polycrystalline silicon. Following the first layer patterning, an additional layer of dielectric is formed on the wafer to form the gate dielectric above channel region 106-1, and above any other areas in the silicon substrate to which the third layer of polycrystalline silicon is to make a gate. These regions can then be implanted to the desired threshold voltage (e.g. approximately 0.5v to 1.5v). The third layer of polycrystalline silicon is for a transistor (ranging from 200Å to 500Å in thickness) then formed and doped to appropriate conductivity, for example 20

ohms/square. Polycrystalline silicon layer 109 is then patterned in order to form word line 109.

Under "Description of Specific Embodiments", please amend the paragraph beginning on page 28, line 12 as follows:

This will therefore require formation of a thick dielectric region as part of the field isolation process protecting the substrate in the space between the poly 2 word lines. This can be accomplished by using a process as described in U.S. Patent Application Serial No. 323,779, filed March 15, 1989, and assigned to ~~SunDisk~~ SanDisk, the assignee of this application. This is actually forming trench isolation, but with BN+ abutting this trench, we may experience severe junction leakage as well as loss of a portion of the BN+ conductor. This cell of this second embodiment is attractive because it is double poly, low programming current, very fast programming, programming away from drain junction, small and scalable cell. Cell size is quite attractive as indicated below for three representative geometries:

1.0m geometries: cell = 4.0 X 2.0 = $8.0m^2$

0.8m geometries: cell = 3.2 X 1.6 = $5.2m^2$

0.6m geometries: cell = 2.3 X 1.2 = $2.8m^2$

Under "Description of Specific Embodiments", please amend the paragraph beginning on page 34, line 3 as follows:

In one embodiment, rather than the use of 100Å tunneling oxide for the erase operation as in the prior art Ma approach, a thick oxide, geometrically enhanced, poly-to-poly tunneling approach is used, as shown for example in Figures 9a and 9b, where the poly3 word line serves the dual function of cell selection and erase anode (one of the architecture/operational approaches taught in the above-mentioned ~~SunDisk~~ SanDisk Patent No. 5,313,421). Figures 10a and 10b shows the equivalent circuit of this cell/array and TABLE 4 summarizes its operation.

Under "Description of Specific Embodiments", please amend the paragraph beginning on page 44, line 6 as follows:

Form field oxide 1100 to a thickness of about 1500Å, and etch it into horizontal strips, adding appropriate channel/field implants prior to or at this step. Use an oxide spacer approach to reduce channel width (for example, reduce from about 0.25μ as etched to about 0.1μ post spacer formation, thereby improving control gate coupling). Grow floating gate oxide 1101, (approximately 300Å gate oxide). As shown in ~~SunDisk~~ SanDisk U.S. patent 5,343,063, the fabrication steps up through the forming of poly1 1102 to a thickness of about 1500Å are performed. Poly1 is then etched into horizontal strips overlying the channel regions plus generous overlap on the field region to either side of the channel. As with channel width, a spacer approach can be used to decrease the etched poly1 spacing, thereby increasing net poly1 overlap of field oxide, or "wings". For example, after the spacer step, poly1 spacing is reduced to about 0.1μ, giving poly1 wings of about 0.15μ per side - refer to Figure 11b showing a cross-section through the channel along the column direction for an example of poly1 wings over field oxide. Note that because of the narrow channel widths vis a vis the poly1 thickness, poly1 1102 will completely fill the trench, resulting in a substantially planar surface. Next form thin ONO 1103 (for example, having about 200Å tox effective) on top of and along edges of the poly1 strips. In an alternative embodiment, a portion of the top film is formed as part of an initially deposited poly1 layer stack.

Under "Description of Specific Embodiments", please amend the paragraph beginning on page 44, line 31 as follows:

Referring to Figures ~~12a(i) and 12a(ii)~~ 12a-1 and 12a-2, deposit a sandwich layer of poly2 1104 (about 1500Å), thick poly3/2 isolation oxide 1105 (approximately 2000Å), plus a sufficiently thick etch stopping layer 1106 (to block underlying oxide removal when exposed to oxide type etch), and top oxide layer 1107. Using a patterned photoresist masking layer 1108, these are then etched in strips along the column direction, down to the poly1 layer, to form poly2 the steering gate lines. These exposed poly1 regions are overlying the areas to become select channel and BN+.

Under "Description of Specific Embodiments", please amend the paragraph beginning on page 45, line 6 as follows:

Referring to Figures ~~12b(i) and 12b(ii)~~ 12b-1 and 12b-2, strip previous photoresist and pattern new photoresist layer 1109 to cover and protect exposed poly1 over the select channel regions. Etch exposed poly1 1102 and all its underlying oxide 1101 which cover the to-be-formed BN+ regions. Oxide layer 1107 over etch stopping layer 1106 is used to protect etch stopping layer 1106 from being etched by the poly etch as poly1 1102 is being removed. Etch stopping layer 1106 (e.g. thin undoped polysilicon or possibly nitride - must have low etch rate compared to oxide etch rates) is used to prevent that portion of thick poly3/2 isolation oxide 1105 not covered by photoresist 1109 from being etched down as oxide 1101 beneath poly1 1102 is etched away. The oxide etch system used is both highly anisotropic (e.g. RIE) and selective vis a vis the underlying silicon substrate, resulting in negligible etching of that substrate, accommodating the large differences in oxide thicknesses being removed between field oxide (approximately 1500Å) and gate oxide regions (approximately 300Å). Following completion of all etching, photoresist 1109 is removed.

Under "Description of Specific Embodiments", please amend the paragraph beginning on page 45, line 25 as follows:

Referring to Figures ~~12c(i) and 12c(ii)~~ 12c-1 and 12c-2, at this point, an option is to implant and drive a sufficient Boron dose to form a p+ DMOS type doping profile adjacent to the BN+ junction (alternatively, this is the point at which the arsenic BN+ is implanted, but the resulting lateral diffusion makes the floating gate channel unnecessarily short). As shown in Figs. ~~12c(i) and 12c(ii)~~ 12c-1 and 12c-2, oxide is formed and reactive ion etched back down to silicon to form sidewall spacers 1110 (about 750Å thick, with the thickness here being determined by interpoly3/2 erase high voltage isolation requirements, for example, about 25v). The arsenic BN+ strips are then implanted.

Under "Description of Specific Embodiments", please amend the paragraph beginning on page 46, line 3 as follows:

Referring to Figures ~~12d(i) and 12d(ii)~~ 12d-1 and 12d-2, a new patterned photoresist layer 1111 is added to cover and protect BN+ strips. The exposed poly1 over channel strips is

etched, to expose the selected channel regions. (Since some of the poly1 overlies channel regions and is therefore thicker, while other portions overlie field oxide and is thinner, the same considerations for oxide etch selectivity apply as above, in the oxide over BN+ etching case.)

Under "Description of Specific Embodiments", please amend the paragraph beginning on page 46, line 11 as follows:

Referring to Figures ~~12e(i) and 12e(ii)~~ 12e-1 and 12e-2, once photoresist 1111 is stripped, oxide is formed (e.g. via thermal oxidation or some composite oxide) to simultaneously form the poly1 sidewall 1112 and corner interpoly3/1 tunneling oxides 1113 (for example, about 350Å), the poly3 gate oxide 1114 over the select channel and oxide 1115 over BN+ (e.g. less than about 300Å - the requirement for both of these oxides being they must be sufficiently thick to reliably hold up to the erase voltage to substrate differential). A select transistor threshold adjust implant can be optionally introduced at this time (e.g. increasing channel dopant concentration to raise select Vt, or introducing compensation implant to reduce select Vt).

Under "Description of Specific Embodiments", please amend the paragraph beginning on page 46, line 23 as follows:

Referring to Figures ~~12f(i) and 12f(ii)~~ 12f-1 and 12f-2, after deposition and patterning of poly3 (which in one embodiment is polysilicide in order to reduce word line delay) the basic dual gate cell structure is complete. In one embodiment of this invention, a high electrical field region is enhanced in the channel far away from the reverse field region located in conventional devices near the drain and source regions. This is achieved, for example, by utilizing regions 1200 of increased doping concentration at the boundary between the channels 1201 and 1202 and transfer channel region 1203. In one embodiment, the width of region 1200 is on the order of 0.1 microns.